Fig. 1
PRIOR ART

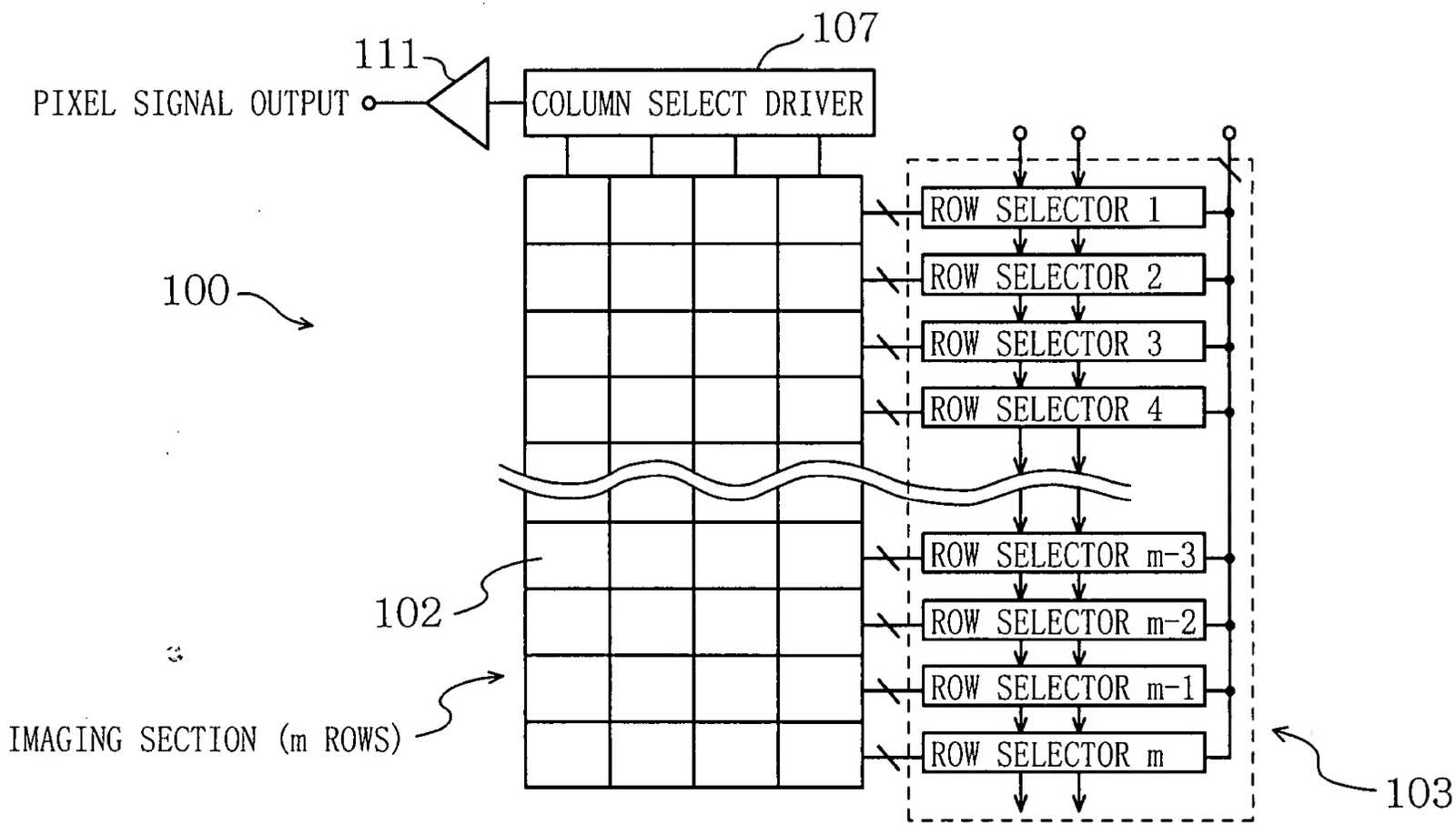


Fig. 2

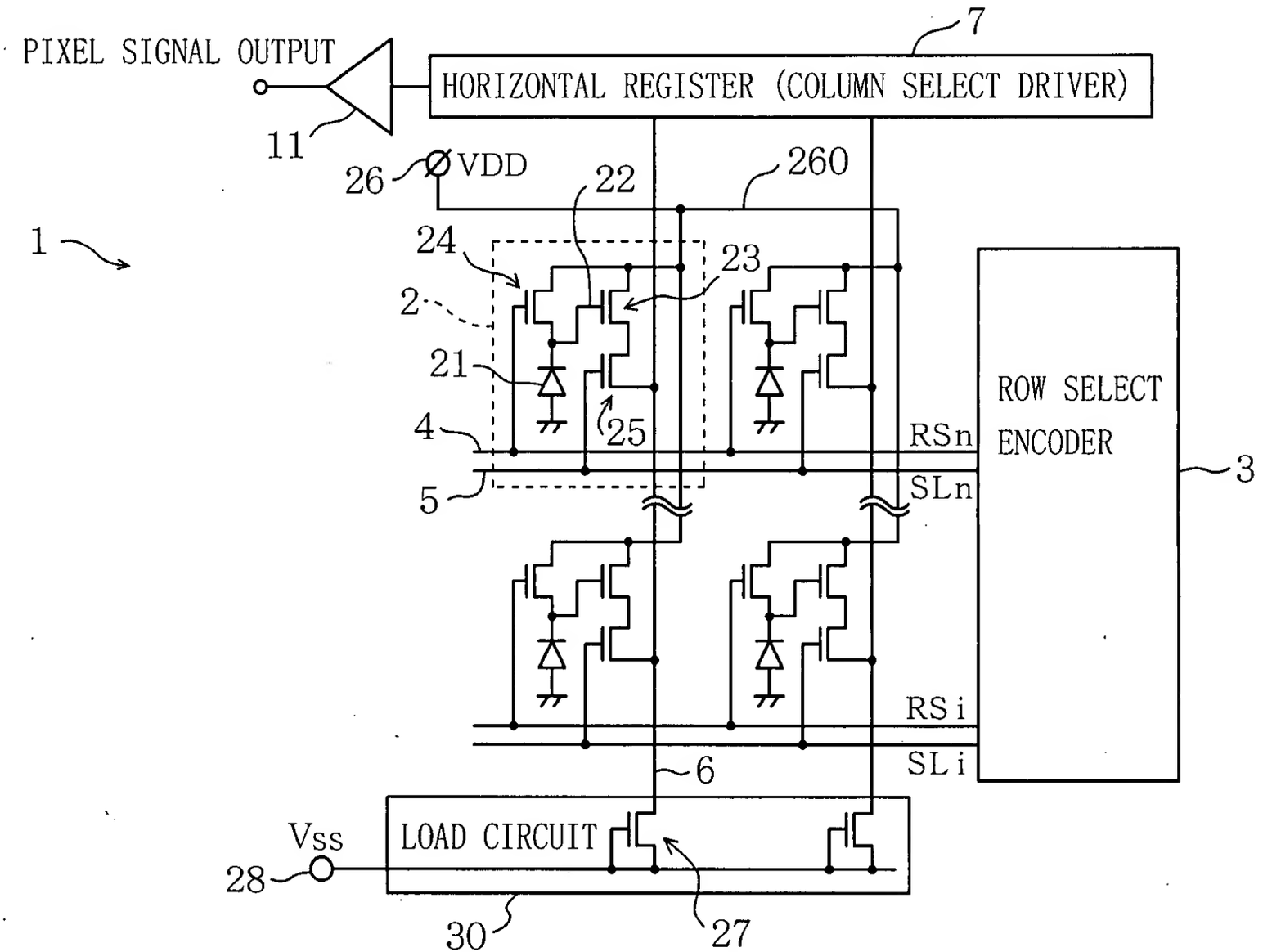


Fig. 3

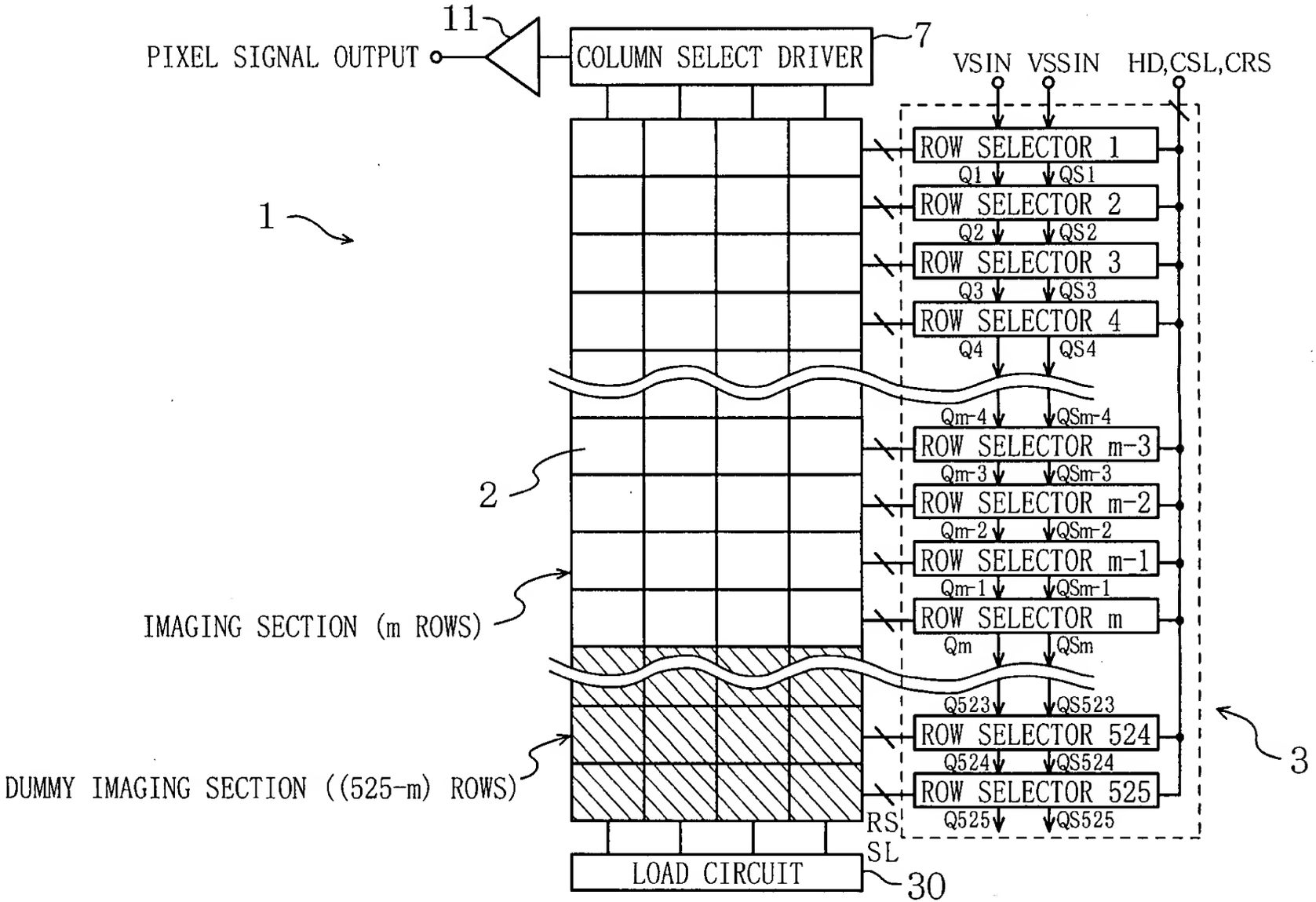


Fig. 4

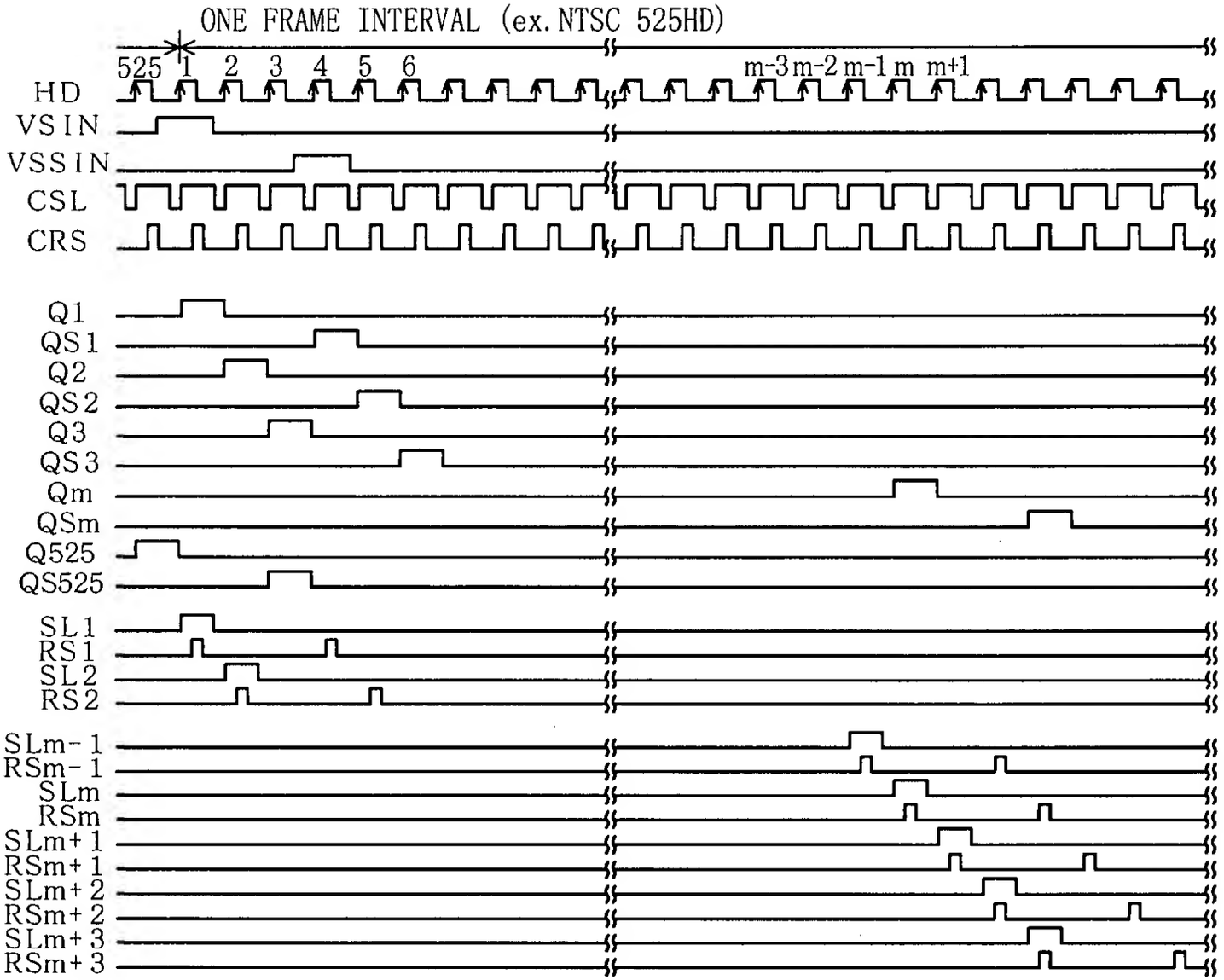

ONE FRAME INTERVAL (ex. NTSC 525HD)
525 1 2 3 4 5 6
m-3 m-2 m-1 m m+1
HD
VSIN
VSSIN
CSL
CRS
Q1
QS1
Q2
QS2
Q3
QS3
Qm
QSm
Q525
QS525
SL1
RS1
SL2
RS2
SLm-1
RSm-1
SLm
RSm
SLm+1
RSm+1
SLm+2
RSm+2
SLm+3
RSm+3

Fig. 5

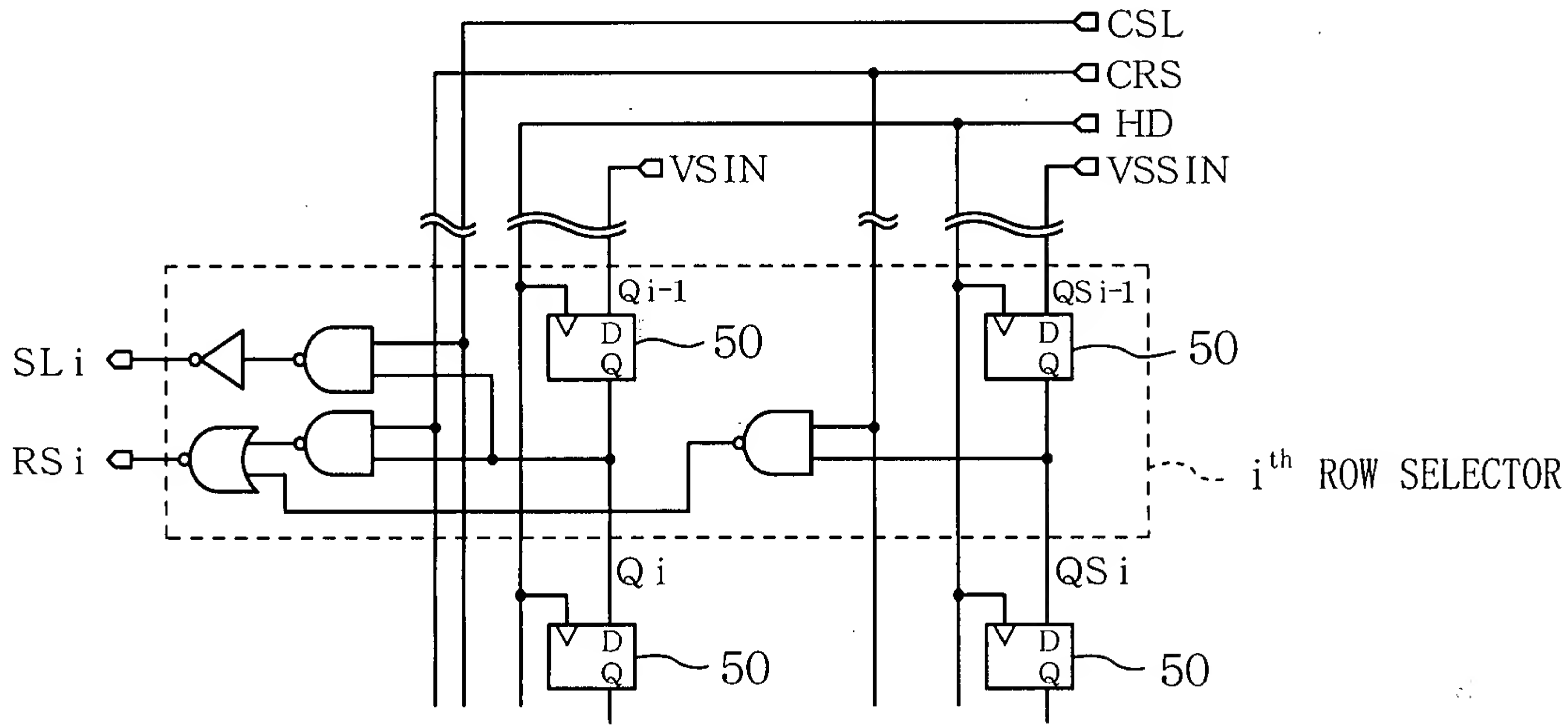

CSL
CRS
HD
VSIN
VSSIN
Q i-1
QS i-1
Q i
QS i
D
Q
50
SL i
RS i
i th ROW SELECTOR

Fig. 6

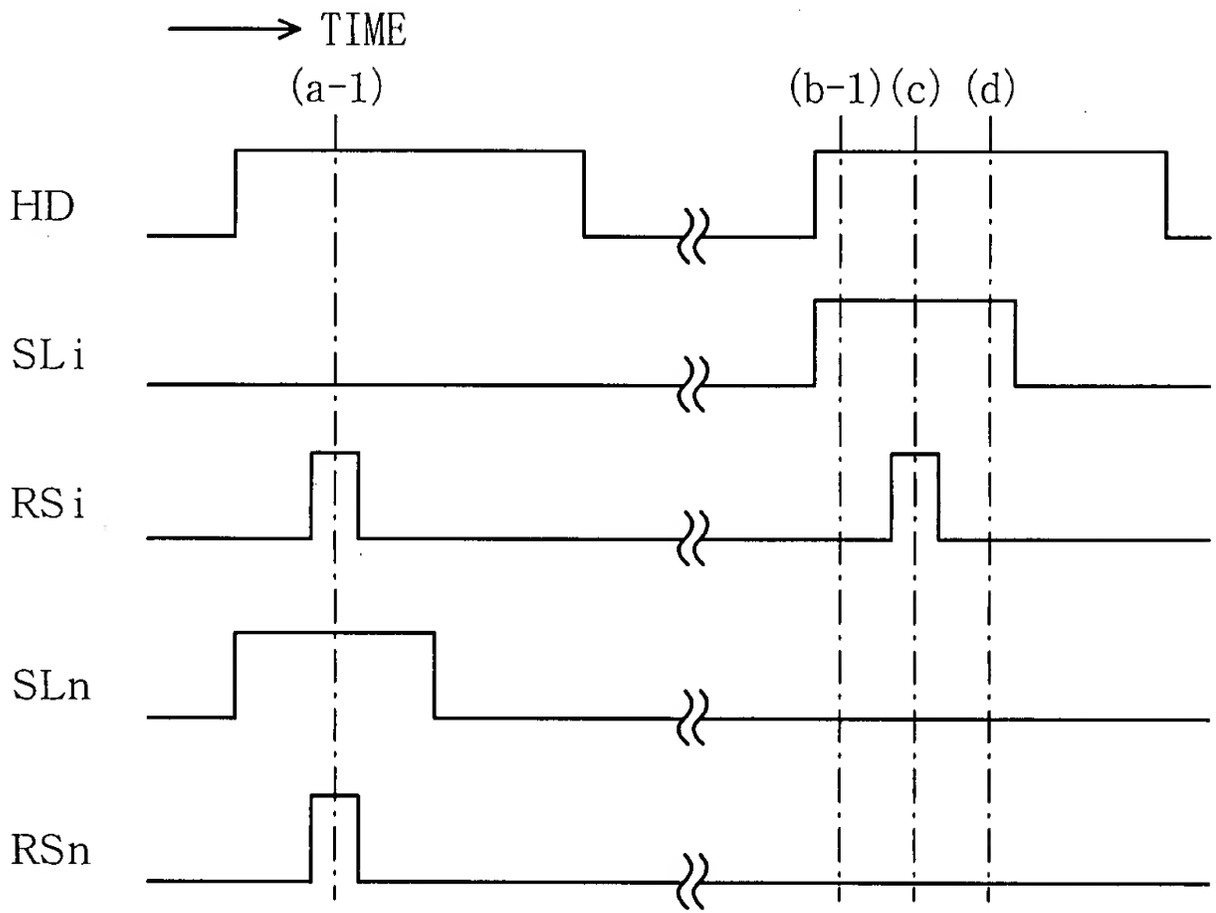


Fig. 7

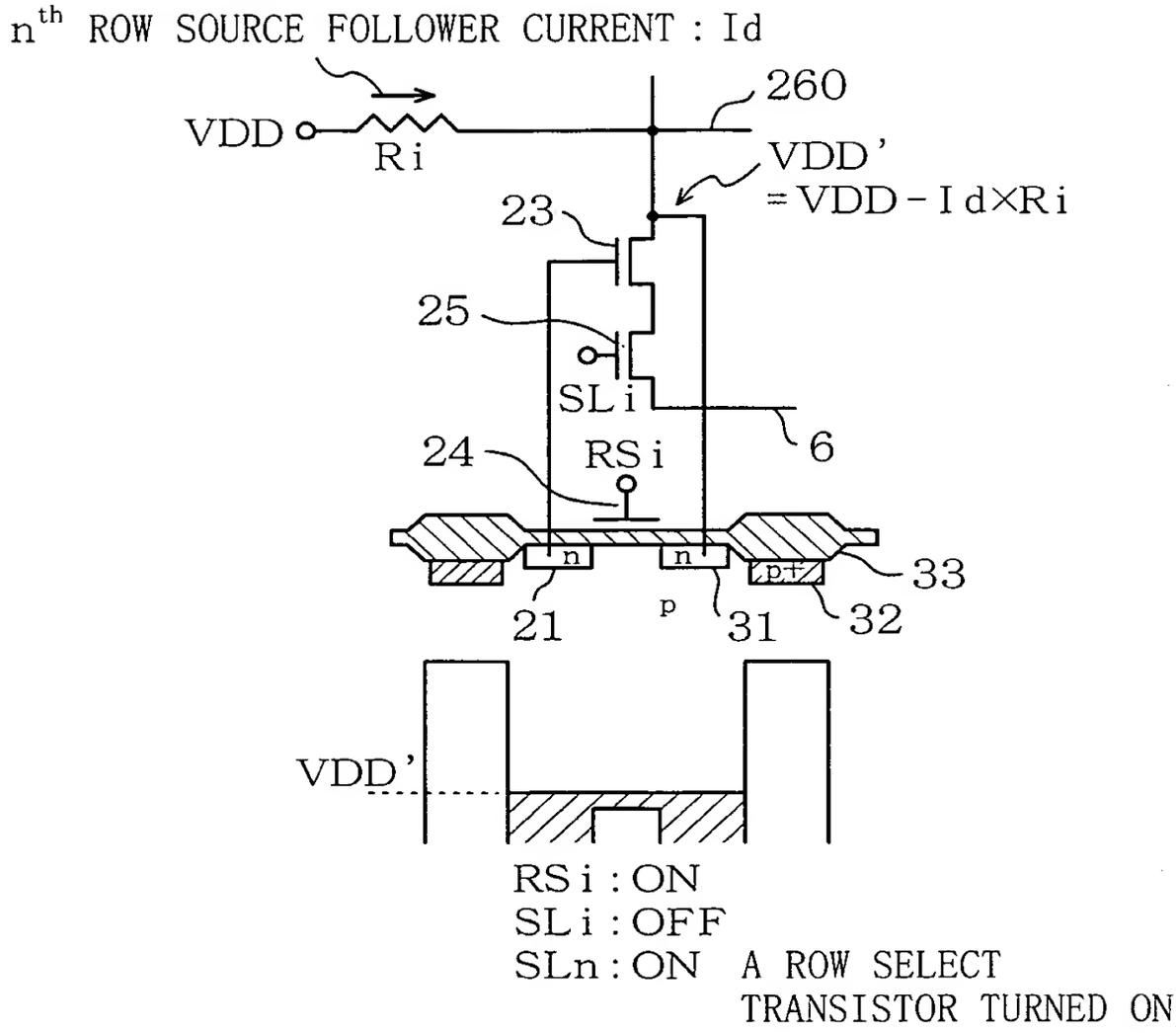

n^th ROW SOURCE FOLLOWER CURRENT : Id
VDD
Ri
260
VDD'
=VDD-Id×Ri
23
25
SLi
6
24
RSi
n
n
p+
33
21
p
31
32
VDD'
RSi : ON
SLi : OFF
SLn : ON A ROW SELECT
TRANSISTOR TURNED ON

Fig. 8

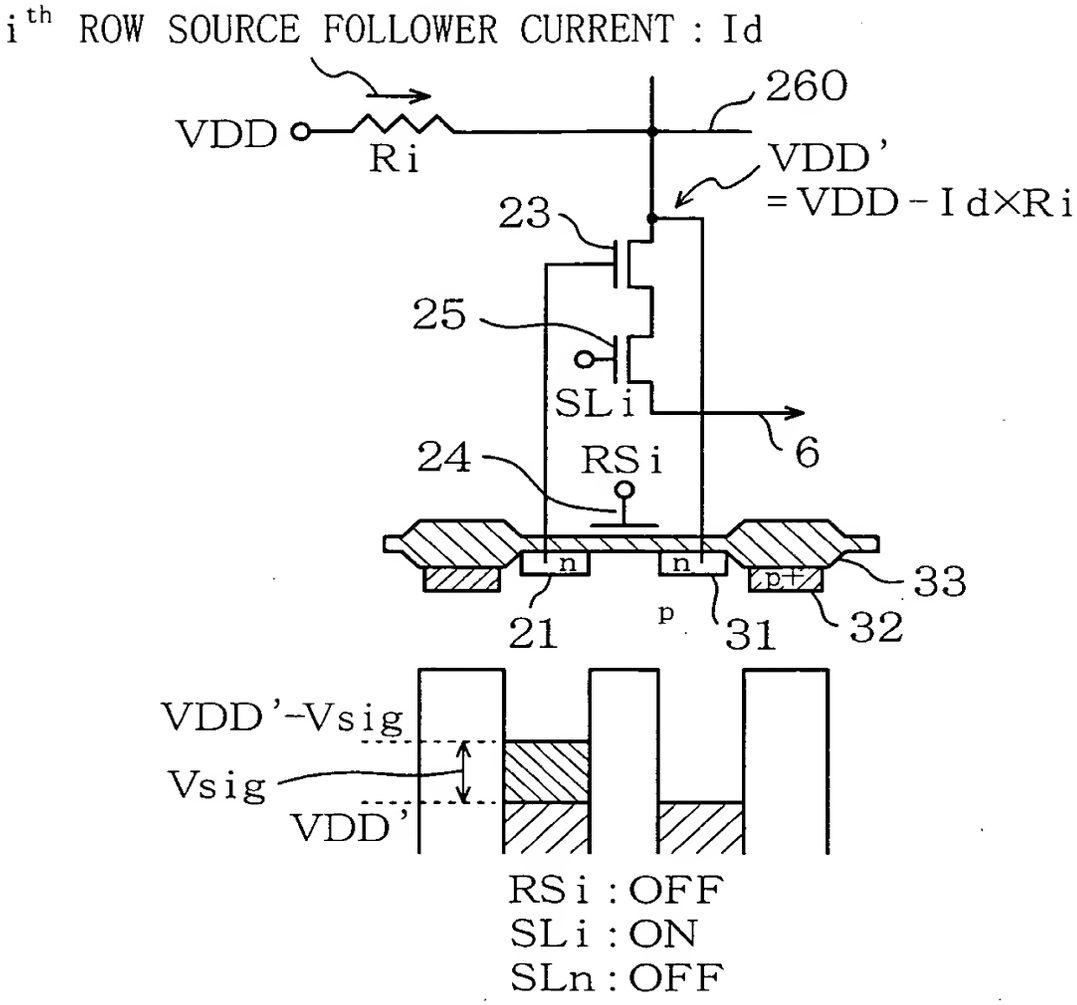

i th ROW SOURCE FOLLOWER CURRENT : Id
VDD
Ri
260
VDD'
=VDD-Id×Ri
23
25
SLi
6
24
RSi
n
n
p+
33
21
p
31
32
VDD'-Vsig
Vsig
VDD'
RSi : OFF
SLi : ON
SLn : OFF

Fig. 9

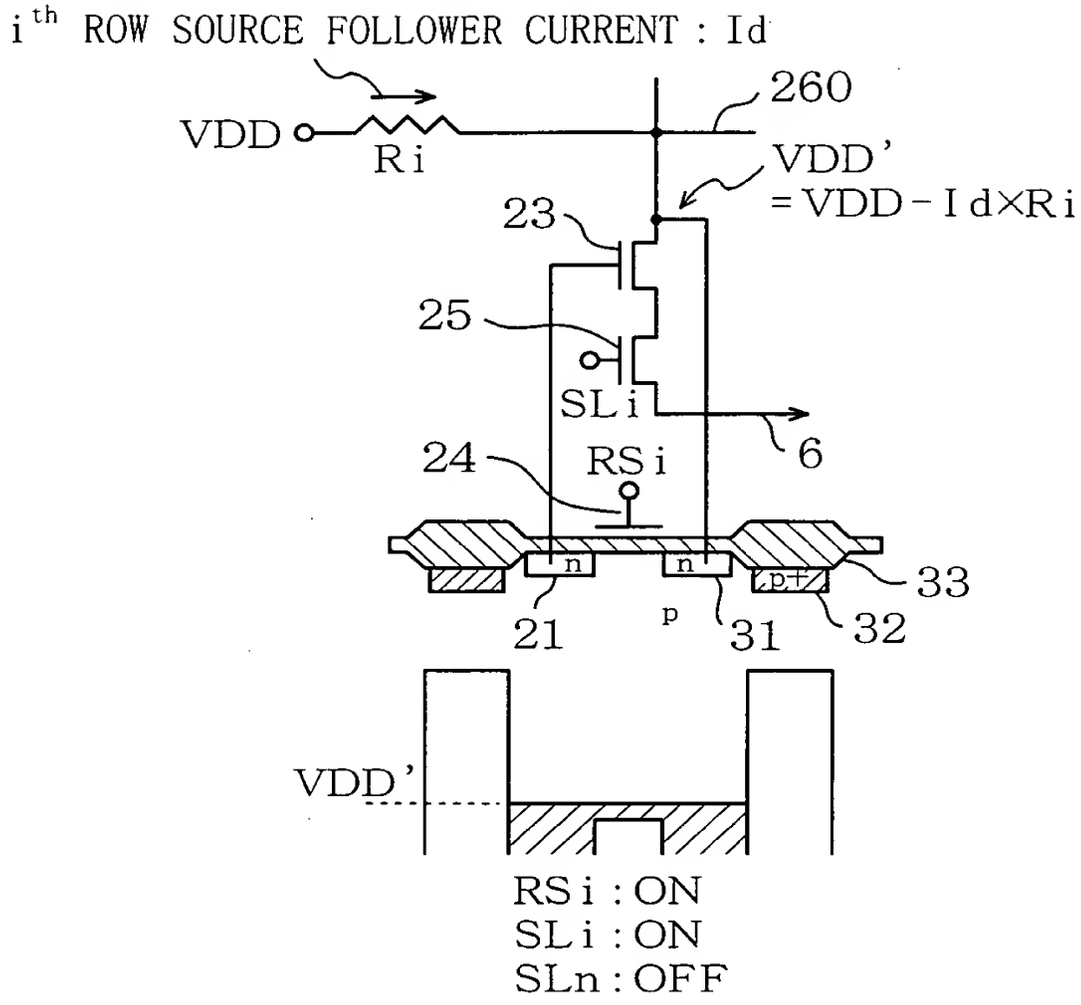

i th ROW SOURCE FOLLOWER CURRENT : Id
VDD
Ri
260
VDD'
=VDD-Id×Ri
23
25
SLi
6
24
RSi
n
n
p+
33
21
p
31
32
VDD'
RSi : ON
SLi : ON
SLn : OFF

Fig. 10

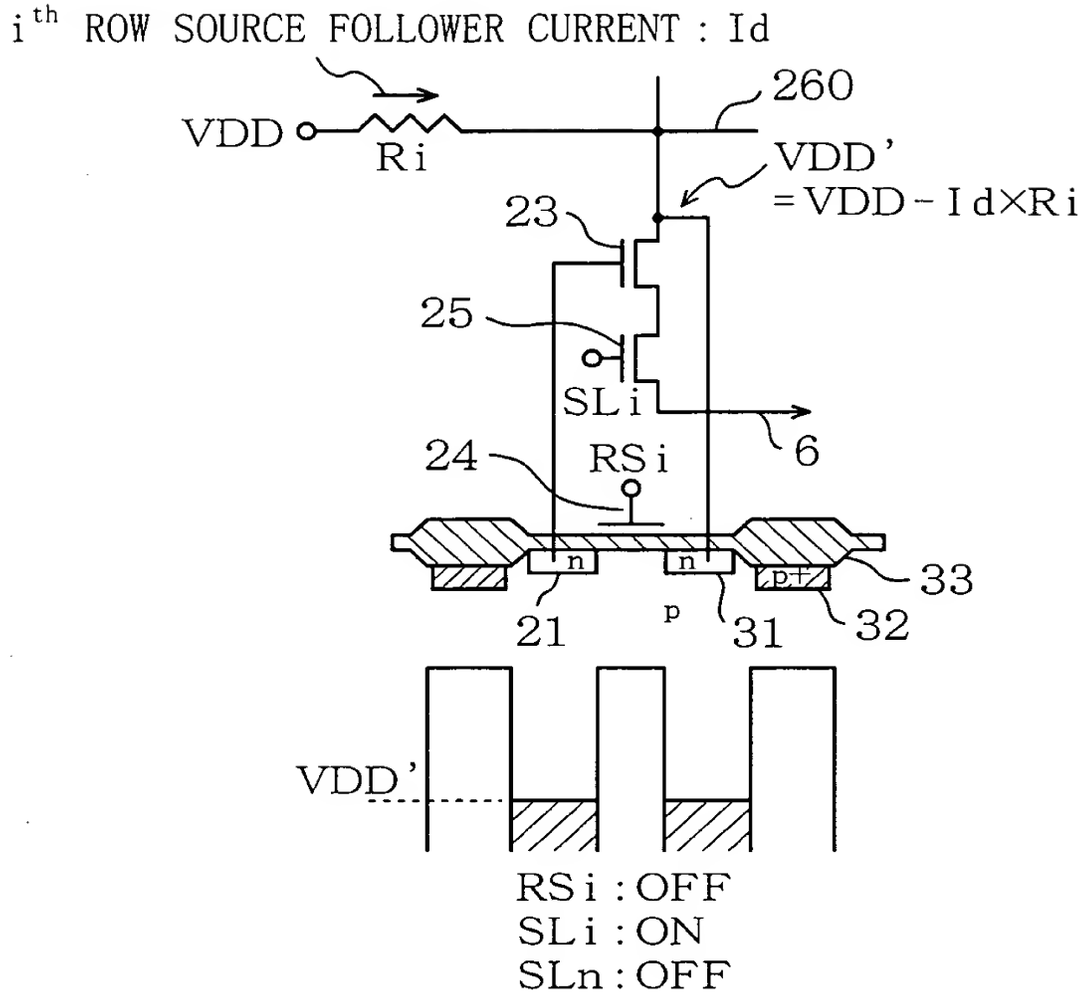

i th ROW SOURCE FOLLOWER CURRENT : Id
VDD
Ri
260
VDD'
=VDD-Id×Ri
23
25
SLi
6
24
RSi
n
n
p+
33
21
p
31
32
VDD'
RSi : OFF
SLi : ON
SLn : OFF

Fig. 11

PRIOR ART

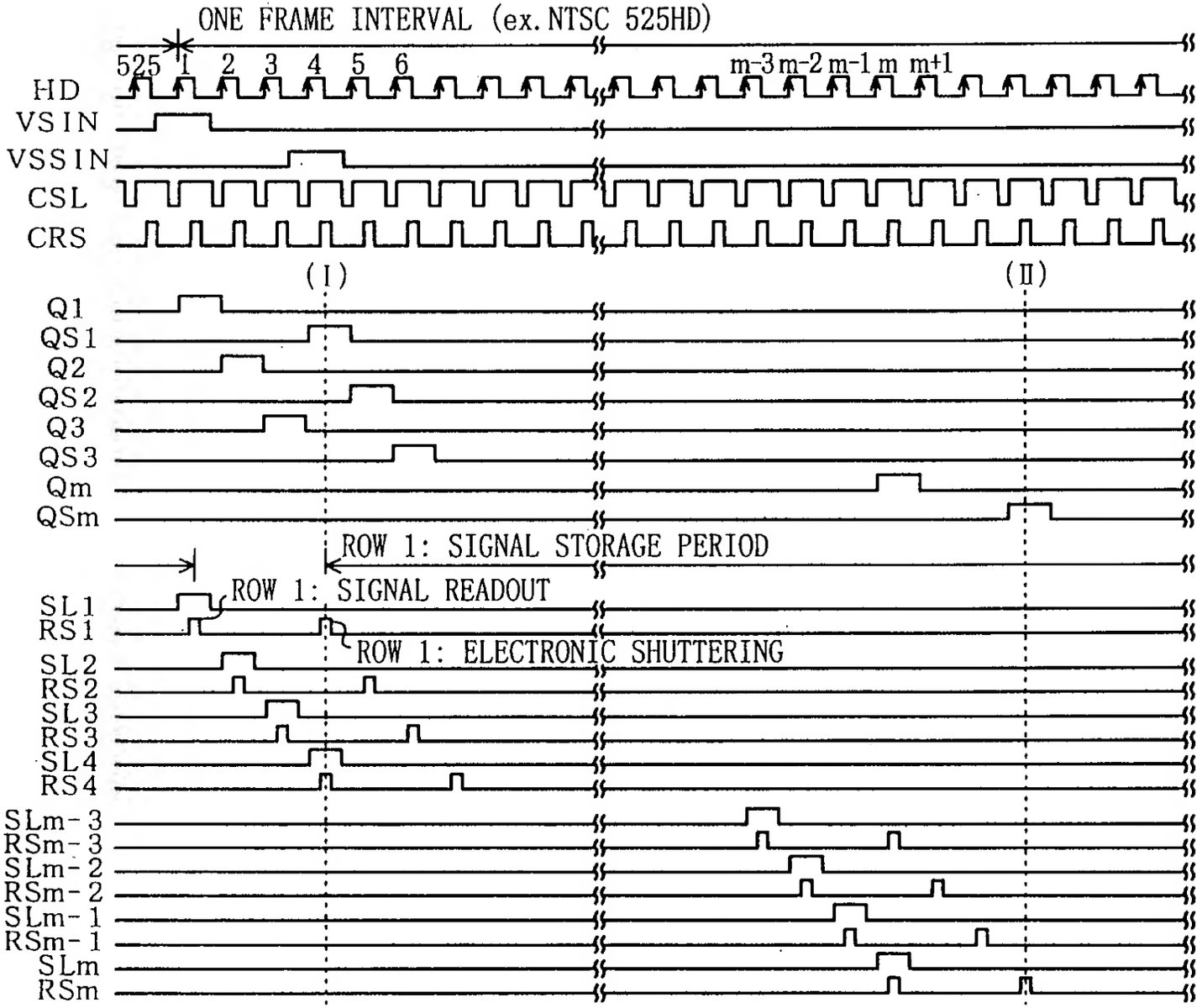


Fig. 12
PRIOR ART

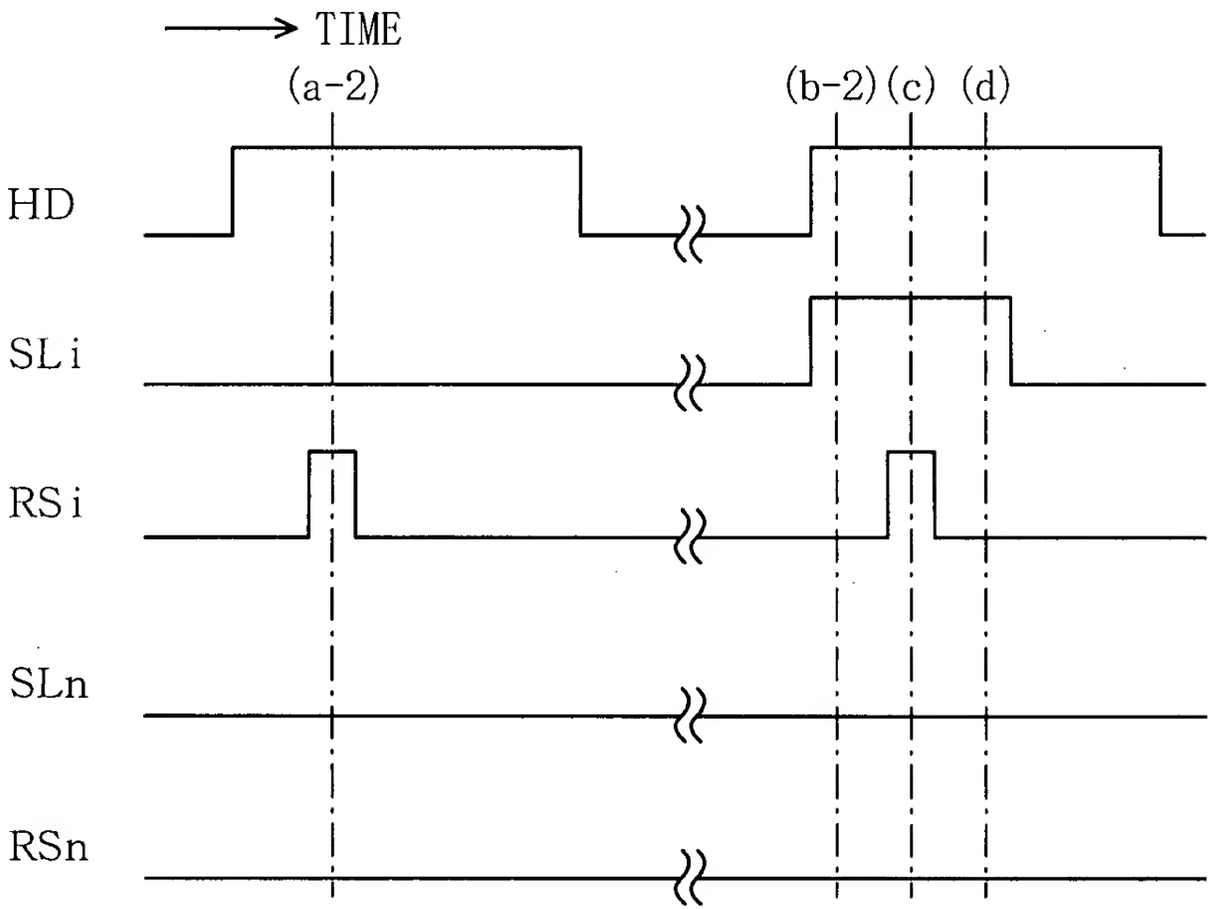
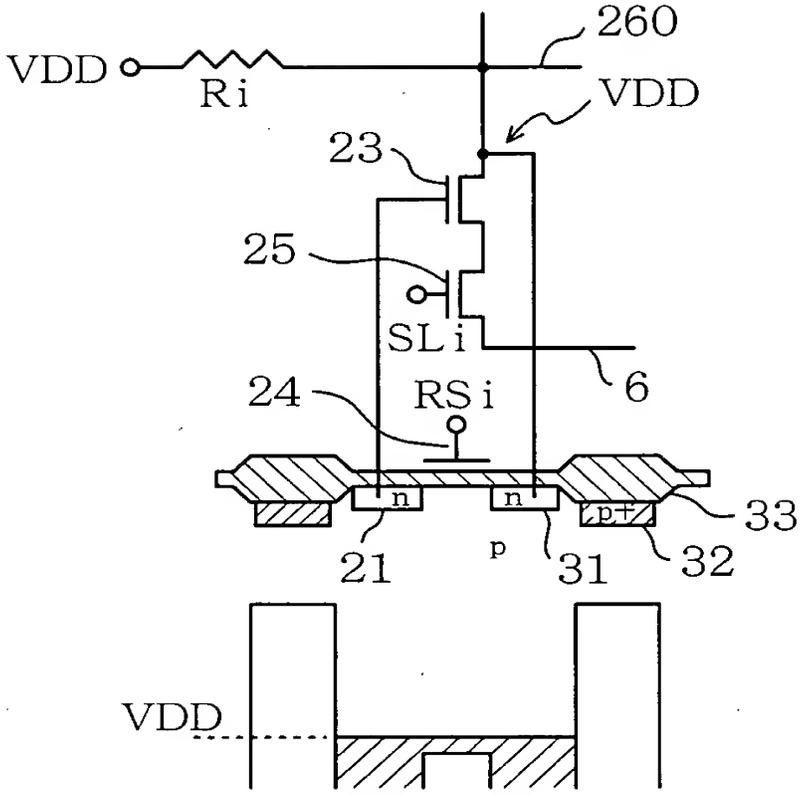


Fig. 13
PRIOR ART



RSi : ON
SLi : OFF
SLn : OFF ALL ROW SELECT
TRANSISTORS TURNED OFF

Fig. 14
PRIOR ART

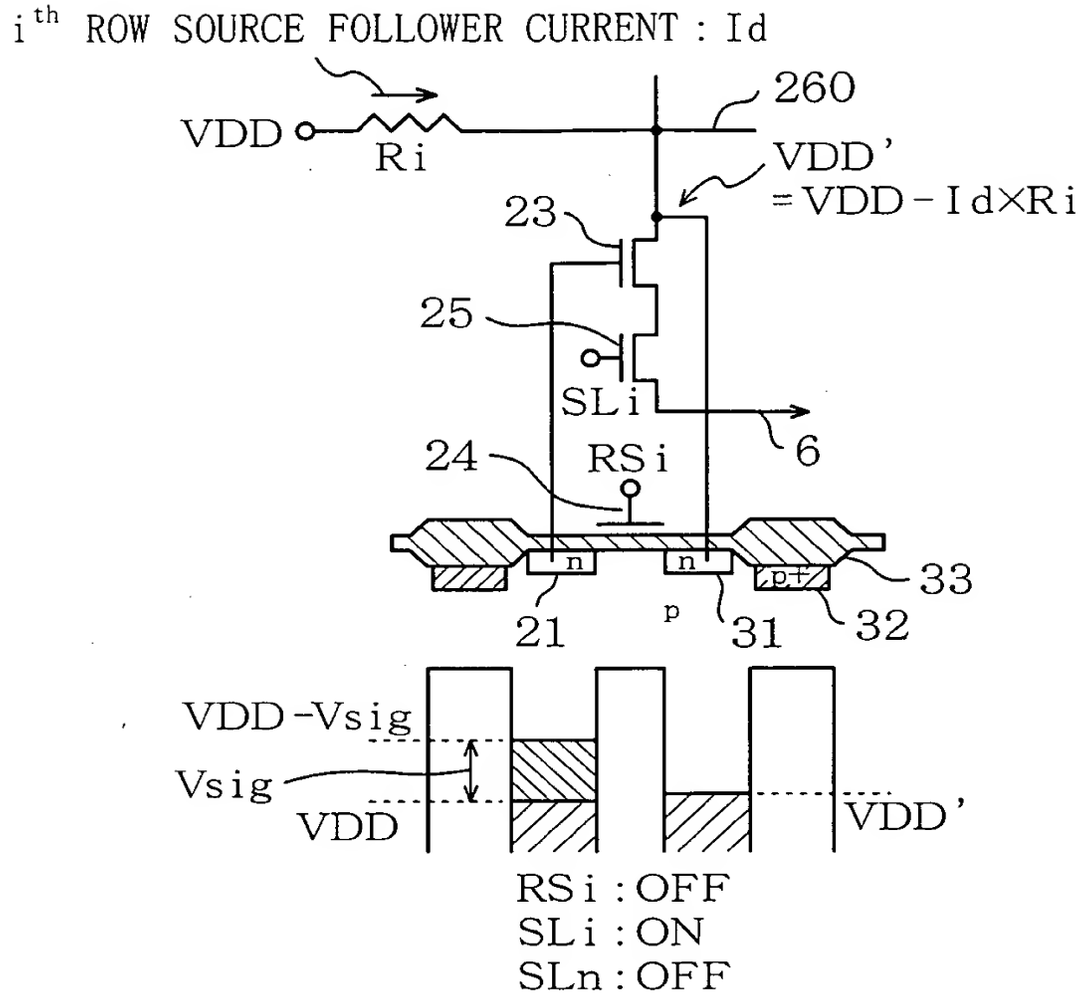


Fig. 15

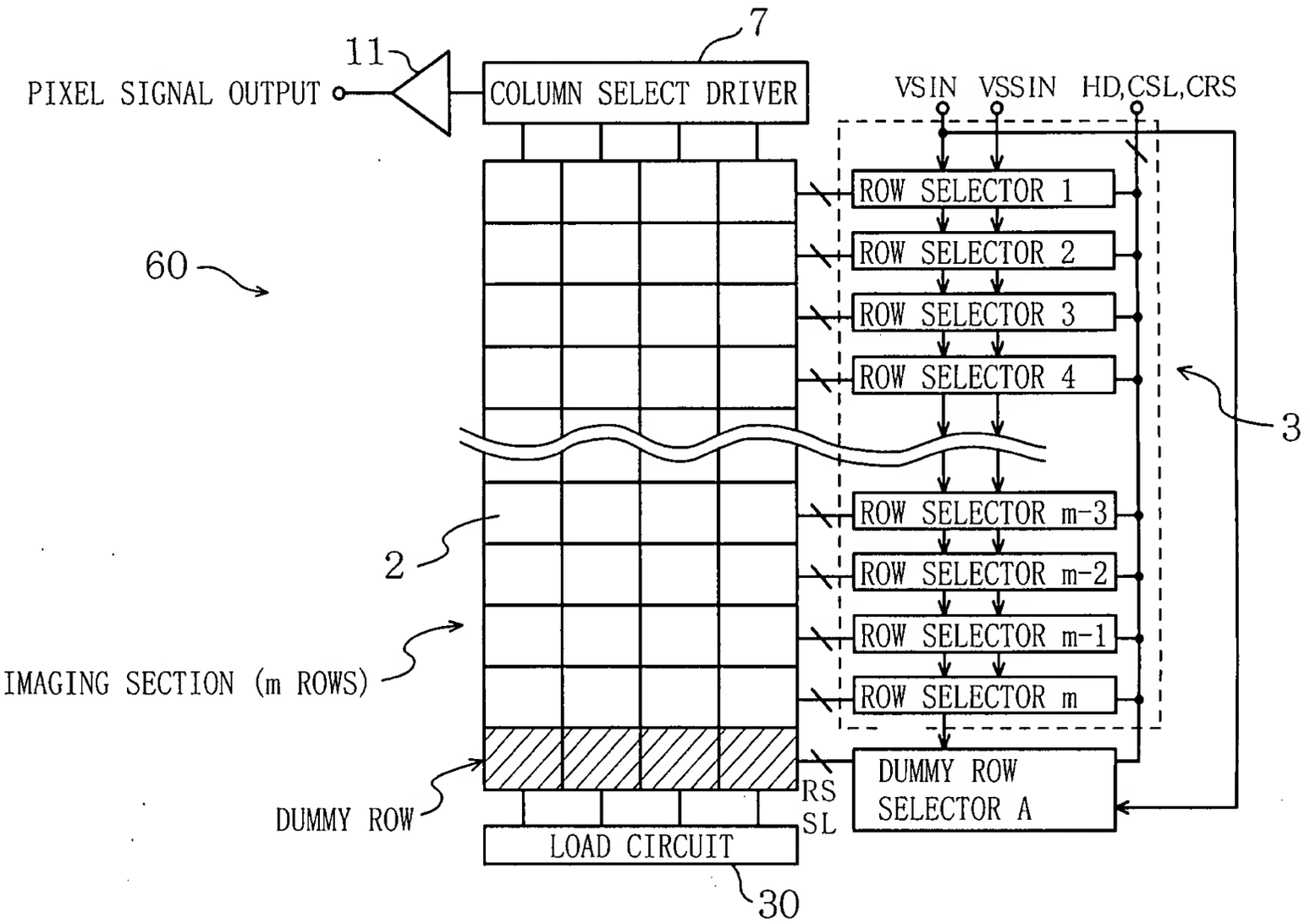


Fig. 16

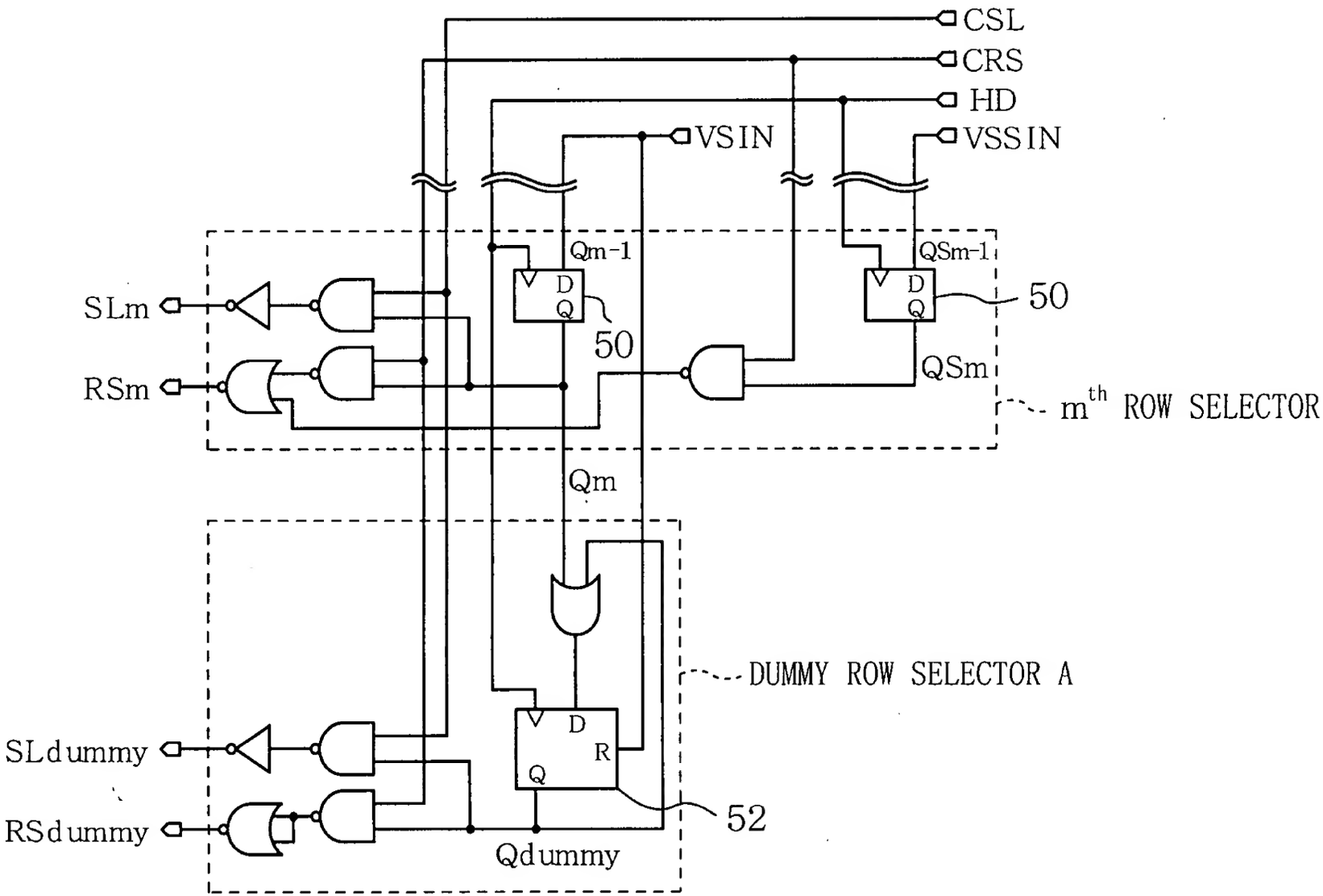

CSL
CRS
HD
VSIN
VSSIN
Qm-1
QSm-1
D
Q
50
SLm
RSm
QSm
m^th ROW SELECTOR
Qm
DUMMY ROW SELECTOR A
SLdummy
RSdummy
D
R
Q
52
Qdummy

Fig. 17

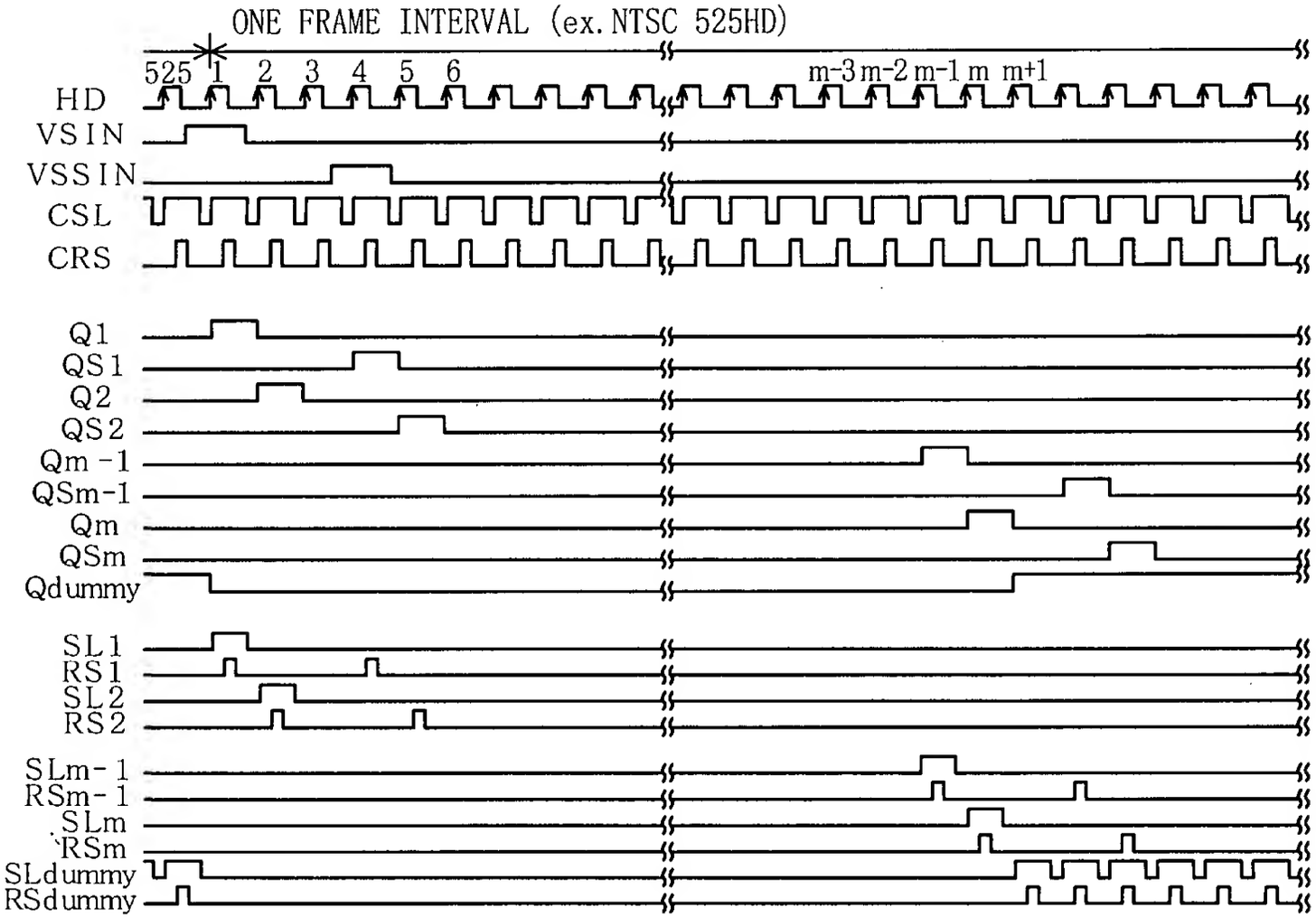

ONE FRAME INTERVAL (ex. NTSC 525HD)
525 1 2 3 4 5 6
m-3 m-2 m-1 m m+1
HD
VSIN
VSSIN
CSL
CRS
Q1
QS1
Q2
QS2
Qm-1
QSm-1
Qm
QSm
Qdummy
SL1
RS1
SL2
RS2
SLm-1
RSm-1
SLm
RSm
SLdummy
RSdummy

Fig. 18

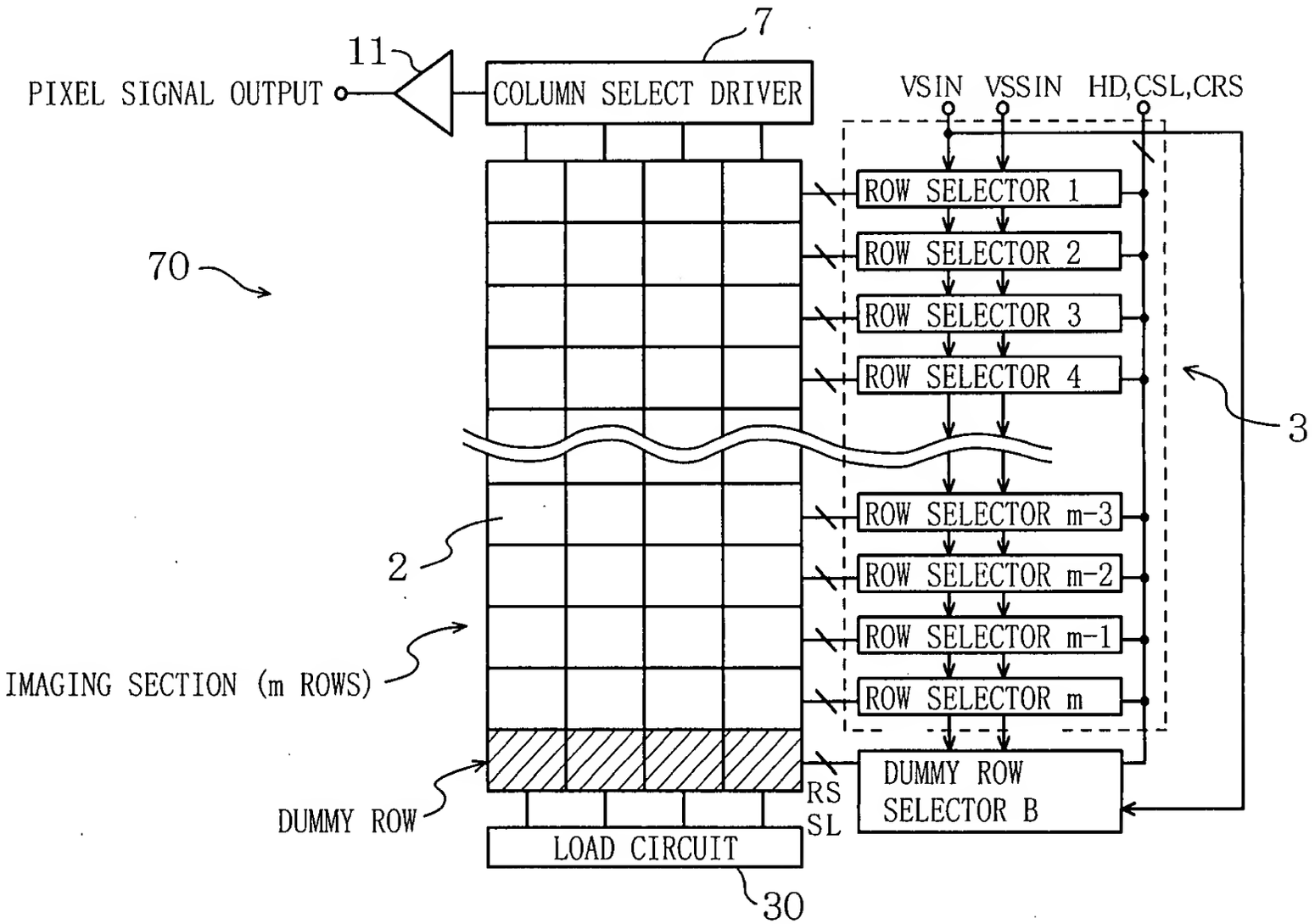


Fig. 19

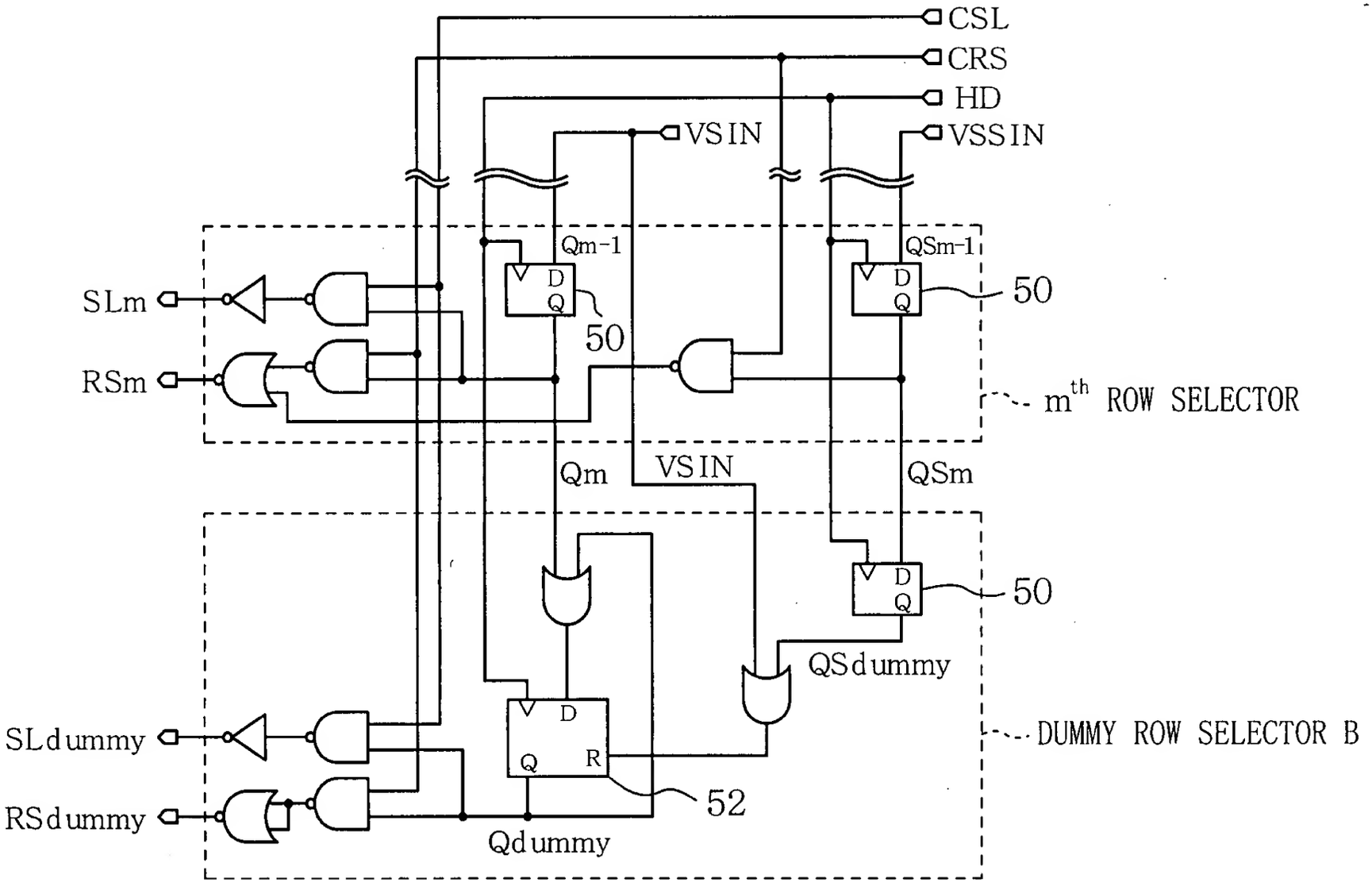

CSL
CRS
HD
VSIN
VSSIN
Qm-1
QSm-1
D
Q
50
SLm
RSm
m^th ROW SELECTOR
Qm
VSIN
QSm
QSdummy
SLdummy
RSdummy
R
52
Qdummy
DUMMY ROW SELECTOR B

Fig. 20

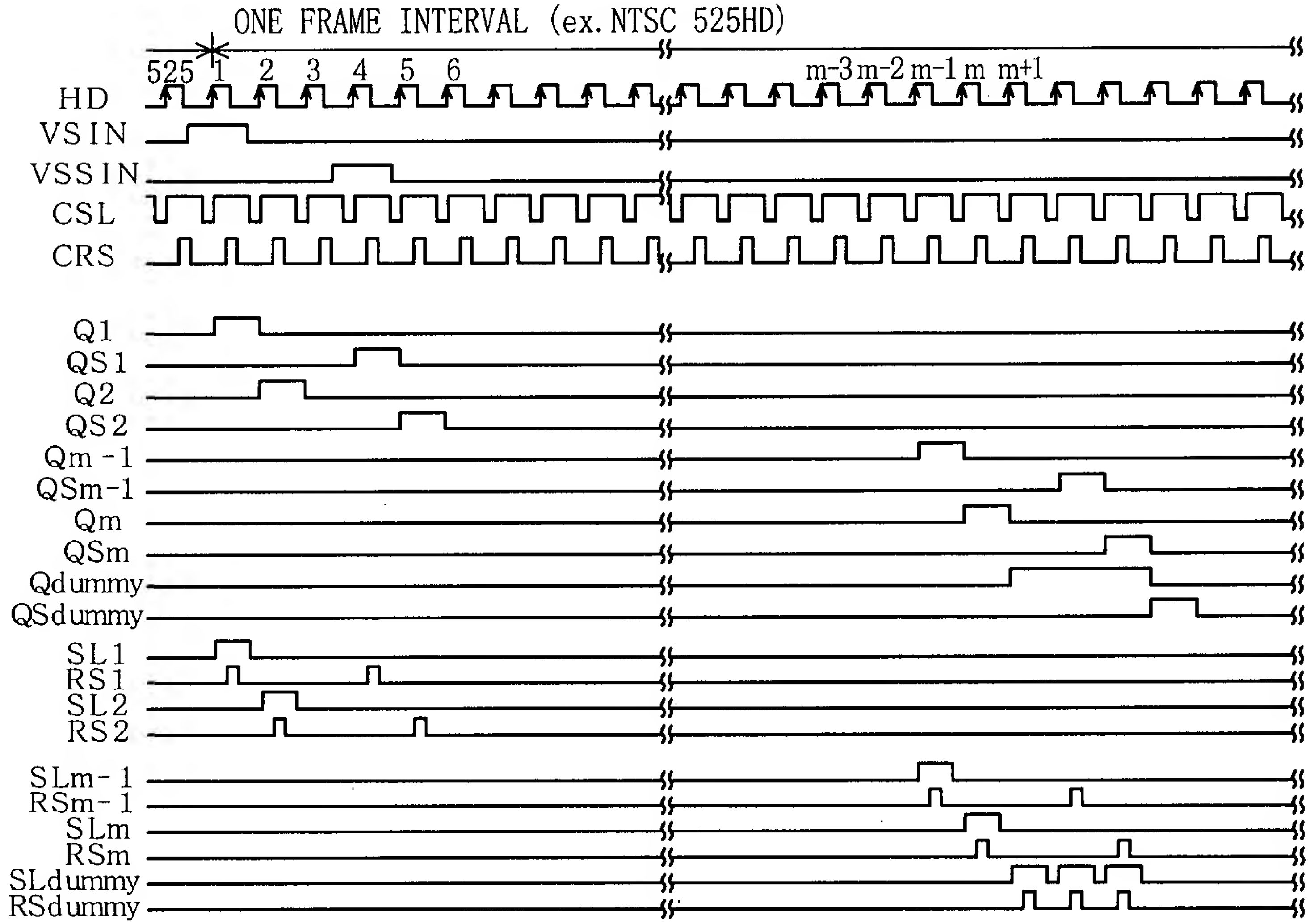

ONE FRAME INTERVAL (ex. NTSC 525HD)
525 1 2 3 4 5 6
m-3 m-2 m-1 m m+1
HD
VSIN
VSSIN
CSL
CRS
Q1
QS1
Q2
QS2
Qm-1
QSm-1
Qm
QSm
Qdummy
QSdummy
SL1
RS1
SL2
RS2
SLm-1
RSm-1
SLm
RSm
SLdummy
RSdummy

Fig. 21